Notice of Allowability	Application No.	Applicant(s)	
	09/630,348	HSU ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *January 14, 2005*.

2. ☒ The allowed claim(s) is/are *2-19*.

3. ☒ The drawings filed on *31 July 2000* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 7/31/2000
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Clean copy of Allowed claims*.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' petition dated January 14, 2005 and communication dated June 1, 2004. Claims 1, 2, 6, 9-11 and 13-16 were amended. Claims 1-19 of the application are pending.

Drawings

2. The drawings submitted on July 31, 2000 are accepted.

Examiner's Amendment

3. Authorization for this examiner's amendment was given in a telephone conversation by Mr. Daniel Bedell on August 9, 2005.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

4. In the amendment to the specification for the Paragraph beginning on Page 20, Line 33:

In Lines 16 to 19, "The system therefore need only investigate function response to only 25 (32) input variable combinations in stead of 2_{21} (2,097,152) possible input variable combinations."

has been changed to

--The system therefore need only investigate function response to only 2^5 (32) input variable combinations in stead of 2^{21} (2,097,152) possible input variable combinations.--

5. In Claim 1:

Delete claim 1.

In Claim 2:

Replace claim 2 with:

2. An apparatus for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior occurring during clock cycles 1 through N of a clock signal following an antecedent event, wherein N is an integer greater than 0, wherein the circuit responds to input signals by producing output signals, wherein the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is production of a second. state change pattern in at least one of the output signals, the apparatus comprising:

a circuit simulator for implementing a simulated circuit, wherein the simulated circuit simulates the circuit described by the circuit specification, wherein the circuit simulator produces

output waveform data representing time-varying behavior of the input and output signals and representing a current state of the simulated circuit;

detector means for detecting in the output waveform data an occurrence of a data pattern representing the antecedent event; and

means for generating a temporally expanded model of the simulated circuit based on the circuit specification and on a state of the circuit upon the occurrence of data pattern as indicated by the output waveform data, the temporally expanded model representing the circuit as a set of N circuit functions CKT_1-CKT_N, each corresponding to a separate one of the N clock cycles and each representing behavior of the circuit during its corresponding clock cycle.

In Claim 8:

Replace claim 8 with:

8. A method for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior occurring during clock cycles 1 through N of a clock signal following an antecedent event, wherein N is an integer greater than 0, wherein the circuit responds to input signals by producing output signals, wherein the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is production of a second state change pattern in at least one of the output signals, the method comprising the steps of:

a. simulating behavior of the circuit described by the circuit specification to produce output waveform data representing time-varying behavior of the input and output signals and representing a current state of the simulated circuit;

b. generating a temporally expanded model of the simulated circuit based on the circuit specification and on a state of the circuit upon the occurrence of data pattern as indicated by the output waveform data, the temporally expanded model representing the circuit as a set of N circuit functions CKT_1-CKT_N, each corresponding to a separate one of the N clock cycles and each representing behavior of the circuit during its corresponding clock cycle.

In Claim 11:

Replace claim 11 with:

11. The method in accordance with claim 10 further comprising the step of:

c. receiving and analyzing the second output variable of each of the circuit functions to verify whether the circuit exhibits the consequent behavior.

In Claim 14:

Replace claim 14 with:

14. An apparatus for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior following an antecedent event, wherein the circuit responds to input signals by producing output signals, wherein the antecedent event is

a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is a second state change pattern in at least one of the output signals, the apparatus comprising:

a circuit simulator for implementing a simulated circuit, wherein the simulated circuit simulates the circuit described by the circuit specification, wherein the circuit simulator produces output waveform data representing time varying behavior of the input and output signals and representing a current state of the simulated circuit;

detector means for detecting in the output waveform data an occurrence of a data pattern representing the antecedent event;

means for generating a state space model of the simulated circuit representing states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output waveform data within a finite number of clock signal cycles after the detector means detects the data pattern representing the antecedent event; and

means for analyzing the state space model to verify the circuit exhibits the consequent behavior.

In Claim 17:

Replace claim 17 with:

17. A method for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior following an antecedent event, wherein the circuit responds to input signals by producing output signals, wherein the antecedent event is a first state

change pattern in at least one of the input and output signals, and wherein the consequent behavior is a second state change pattern in at least one of the output signals, the method comprising the steps of:

simulating the circuit to produce waveform data representing successive state changes of the input and output signals and representing successive states of the circuit;

generating a state space model of the simulated circuit representing states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output waveform data within a finite number of clock signal cycles after the detector means detects the data pattern representing the antecedent event; and

analyzing the state space model to verify the circuit exhibits the consequent behavior.

In Claim 18:

Replace claim 18 with:

18. The method in accordance with claim 17 wherein the circuit transitions between states only on edges of a periodic clock signal supplied as input thereto,

wherein the consequent behavior occurs during the finite number of periods of the clock signal following the antecedent event.

In Claim 19:

Replace claim 19 with:

19. The method in accordance with claim 17 wherein the generated state space model includes only states of the circuit that are reachable from the current state of the circuit represented by the waveform data within the finite number of clock signal cycles after the waveform data represents the antecedent event.

A clean copy of the amended claims is attached.

Reasons for Allowance

6. Claims 2-19 of the application are allowed over prior art of record.

7. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) An electronic circuit verification system including an HDL simulator and a circuit simulation verifier that pass control back and forth between each other; the verifier specifies conditions under which the HDL simulator is to stop simulation of the circuit and specifies the input signal waveforms to be used by the HDL simulator; the circuit simulation verifier receives the signal waveforms generated by the HDL circuit simulator for the specified watched signals and determines whether the watched signals meet the operational correctness and/or performance criteria within specified time limits (**Kasuya,** U.S. Patent 5,905,883);

(2) a functional verification system for verifying the function of cycle based integrated circuit design; the IC is divided into a plurality of combinatorial blocks connecting sequential elements; a complex target design is divided into a large number of blocks; truth tables corresponding to the divided blocks are computed and stored in random access memory; the output values of the IC design corresponding to the input data values are determined by evaluating the blocks by accessing the truth tables in the memory; each block is evaluated by a single access to the memory (**Ganesan et al.,** U. S. Patent 6,138,266); and

(3) a method and an apparatus for validating high-level specifications of sequential digital systems represented by hybrid models; the high level representation of the system is converted into a direct sum extended finite state machine; an operator or a data file then provides a set of initial configurations of the states and variable values; the method determines the set of configurations reachable from the initial configuration through symbolic execution of the extended finite state machine; by representing the transitional relations of the machine and and-product of Boolean expressions and arithmetic expressions, each class of expressions is processed separately; the symbolic execution produces the set of reachable states; the results may be viewed to determine if the given specification produces unexpected results (**Cheng et al.,** U.S. Patent 5,513,122).

Additional state of the art reviewed and considered by the Examiner is found in U.S. Patent 6,311,293; U.S. Patent 6,496,953; U.S. Patent 5,465,216; U.S. Patent 6,115,763; U.S. Patent 6,484,134; U.S. Patent 5,263,149; U.S. Patent 5,745,501; U.S. Patent 6,321,186; U.S.

Patent 6,339,837; Rabiei et al., "Model order reduction of Large circuits using balanced Truncation", IEEE, 1999; Schlipf et al., "An easy approach to formal verification', IEEE, 1997.

None of these references taken either alone or in combination with the prior art of record discloses an apparatus and a method for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior, specifically including:

"(means for) generating a temporally expanded model of the simulated circuit based on the circuit specification and on a state of the circuit upon the occurrence of data pattern as indicated by the output waveform data, the temporally expanded model representing the circuit as a set of N circuit functions CKT_1-CKT_N, each corresponding to a separate one of the N clock cycles and each representing behavior of the circuit during its corresponding clock cycle".

None of these references taken either alone or in combination with the prior art of record discloses an apparatus and a method for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior, specifically including:

"(means for) generating a state space model of the simulated circuit representing states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output waveform data within a finite number of clock signal cycles after the detector means detects the data pattern representing the antecedent event".

8. Any comments considered necessary by applicants must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

K. Thangavelu
Art Unit 2123
August 9, 2005

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100